REMARKS

Reconsideration of the application in view of the above amendments and the following remarks is requested. Claims 1, 2, 5-7, 9-10, and 13-23 are in this application. Claims 3, 4, 8, 11, and 12 have been cancelled. Claims 1, 5, and 13 have been amended. Claims 18-23 have been added to alternately and additionally claim the present invention.

The Examiner objected to the drawings under 37 CFR §1.83(a) as not showing every feature of the invention in the claims. Specifically, the Examiner argued that the phrase "the layer of first material having a top surface" in claim 1 is not shown in the drawings. Applicant notes that the first layer of material can be read to be, for example, polysilicon layer 320. As shown in FIG. 3A, polysilicon layer 320 has a top surface, although the top surface is not labeled. Thus, to add additional clarity, applicant proposes amending FIG. 3A as shown in red on the attached copy of FIG. 3A to show a top surface 321 of polysilicon layer 320. The specification has also been amended to reflect that the top surface of polysilicon layer 320 is designated by the reference label 321.

The Examiner also argued that the drawings do not show a third layer of material formed on the planarized layer of material as required by claim 10. As a result, applicant proposes adding FIG. 3C as shown in red on the attached copy of FIG. 3C to show the third layer of material. The specification has been amended to reflect this change. The Examiner further argued that the steps of etching the layer of third material as required by claim 11 are not shown in the drawings. Claim 11 has been cancelled.

The Examiner rejected claims 4, 5, 12, and 13 under 35 U.S.C. §112, first paragraph, as containing subject matter not described in the specification as to enable one skilled in the art to make and/or use the invention. Applicant disagrees that claims 4, 5, 12, and 13 lack support in the specification. However, in an effort to further prosecution and provide greater clarity, claims 4 and 12 have been cancelled, and claims 5 and 13 have been amended.

Claim 5 recites, in part,

> "wherein the planarized layer of material has a thickness over the wafer upper level, and
>
> "wherein the layer of first material is formed such that the first lower level lies above the wafer upper level by a value that is equal to or greater than the thickness."

Claim 13 recites similar limitations.

The planarized layer of material can be read to be, for example, planarized polysilicon layer 340. As shown in FIG. 3B, planarized polysilicon layer 340 has a thickness X over the wafer upper level. In addition, FIG. 3A shows that polysilicon layer 320 is formed such that first lower level 322 lies above wafer upper level 314 by a value that is equal to or greater than the thickness X. As a result, claims 5 and 13 are believed to satisfy the requirements of the first paragraph of section 112.

The Examiner rejected claims 1-17 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter that applicant regards as the invention. Specifically, the Examiner indicated that the phrases "the wafer having a top surface," "wafer lower level," and "first material having an upper level" can not be understood because FIG. 3A and the detailed description of FIG. 3A describe wafer 300 as comprehending the entire structure of FIG. 3A. For the reasons set forth below, applicant respectfully traverses this rejection.

Applicant's specification recites, in part,

> "[T]he method utilizes a conventionally processed semiconductor wafer 300 that has a top surface 310. Surface 310, in turn, has a number of substantially-equal lower levels 312 and a number of substantially-equal upper levels 314 that lie above the lower levels 312. As further shown in FIG. 3A, the method begins by depositing a layer of polysilicon 320 on surface 310 [of wafer 300]." [Brackets added.] (See from page 4, line 24 to page 5, line 2 of applicant's specification.)

Thus, applicant's specification does not teach that the entire structure of FIG. 3A is wafer 300. In an attempt to add further clarity, applicant proposes amending FIG. 3A as shown in red on the attached copy of FIG. 3A by repositioning reference numeral 300.

Claim 1 recites, in part,

> "1. A method for forming a planarized layer of material on a processed wafer, the wafer having a top surface, the top surface having a wafer lower level and a wafer upper level that lies above the wafer lower level."

Thus, since applicant's specification provides an example of a wafer (300) that has a top surface (310) with a lower level (312) and an upper level (314) that lies above the lower level (312), applicant can find no basis to support the argument that the above language is unclear. Thus, lacking further direction from the Examiner, the above-noted language of claims 1-17 satisfy the requirements of the second paragraph of section 112.

Applicant's specification also recites, in part,

> "Polysilicon layer 320 is conformally deposited and, as a result, also has a top surface 321 that has a number of substantially-equal lower levels 322 and a number of substantially-equal upper levels 324 that lie above the lower levels 322." (See page 5, lines 2-5 of applicant's specification.)

Further, claim 1 recites:

> "forming a layer of first material on the top surface of the wafer, the layer of first material having a top surface, the top surface of the layer of first material having a first lower level and a first upper level that lies above the first lower level."

Thus, since applicant's specification provides an example of a layer (320) that has a top surface (321) with a lower level (322) and an upper level (324) that lies above the lower level (322), applicant can find no basis to support the argument that the above language is unclear. Thus, lacking further direction from the Examiner, the above-noted language of claims 1-17 satisfy the requirements of the second paragraph of section 112.

The Examiner also noted that the step "forming a layer of second material on the top surface of the layer of second material" is unclear because it is not clear how the second material is formed on the second material. Claim 1 has been amended to correct this inadvertent error, and recites that the second layer is formed on the layer of first material.

The Examiner rejected claims 1-8 and 10-16 under 35 U.S.C. §102(b) as being anticipated by Doan et al. (U.S. Patent No. 5,618,381). The Examiner also rejected claims 9 and 17 under 35 U.S.C. §103(a) as being unpatentable over Doan et al. For the reasons set forth below, applicant respectfully traverses these rejections.

Claim 1 has been amended and recites, in part,

> "chemically-mechanically polishing the layer of second material and the underlying layer of first material with a slurry until the layer of second material is all removed from the layer of first material without changing the slurry to form the planarized layer of material."

In rejecting the claims, the Examiner appears to point to dielectric regions 10 and substrate 12 as constituting the wafer of claim 1, with the top surface of dielectric regions 10 constituting the wafer upper level and the top surface of substrate 12 constituting the wafer lower level. In addition, the Examiner pointed to the formation of tungsten layer 22 on dielectric regions 10 and substrate 12 shown in FIG. 6 of Doan as constituting the step of "forming a layer of first material." The Examiner also pointed to the formation of TEOS layer 60 on layer 22 shown in FIG. 6 of Doan as constituting the step of "forming a layer of second material." The Examiner next pointed to the removal of TEOS layer 60 and tunsten layer 22 as constituting the step of "chemically-mechanically polishing" as required by claim 1.

The Doan reference, however, fails to teach the chemically-mechanically polishing step of claim 1. As disclosed by Doan, tungsten layer 22 and TEOS layer 60 are removed in a two step CMP process where the slurry is changed. FIG. 7 shows the results at the end of the first CMP process where a slurry with a silicon oxide abrasive has been used. FIG. 3 shows the results at the end of the second CMP process where a slurry optimized for tungsten polishing has been used. (See column 4, lines 14-30 of Doan.)

As shown in FIG. 7, Doan teaches that not all of the second layer of material (TEOS 60) is removed at the end of the first CMP process as required by the chemically-mechanically polishing step of claim 1. Thus, the chemically-mechanically polishing step of claim 1 can not be read to be the first CMP process. In addition, the combined two step CMP process can not be read to be the chemically-mechanically polishing step of claim 1 because the slurry is changed between processes.

As a result, the Doan reference fails to teach that all of the second layer of material (TEOS 60) is removed at the end of the second CMP process "without changing the slurry" as required by the chemically-mechanically polishing step of claim 1. Thus, claim 1 is not

anticipated by the Doan reference. In addition, since claims 2, 5-7, 10, and 13-16 depend either directly or indirectly from claim 1, claims 2, 5-7, 10, and 13 -16 are not anticipated by Doan for the same reasons as claim 1.

With respect to claims 10 and 13, the Examiner, pointing to column 5, lines 1-26 of Doan, argued that Doan teaches the step of forming a layer of third material on the planarized layer of material.

Claim 10 recites, in part.

> "forming a layer of third material on the planarized layer of material."

As noted above, Doan teaches that FIG. 3 shows the structure that results following the second CMP process. (See column 4, lines 29-31 of Doan.) In column 5, lines 17-26, Doan also teaches that to form a protruding plug, the material surrounding the plug can be removed with a CMP process to expose the plug. This allows for improved contact with a subsequent layer of material, such as sputtered aluminum.

Although the Examiner did not identify what constitutes the third layer of material, the subsequently formed layer of sputtered aluminum can not be read to be the third layer of material required by claim 10 because the sputtered aluminum is not formed on a planarized layer of material, but instead is formed on protruding plugs. As a result, claims 10 and 13 are not anticipated by the Doan reference for this additional reason.

With respect to claim 9, the Examiner argued that it would be obvious to determine a selectivity in the range of 0.9-1.1 in view of Doan. Applicant notes, however, that Doan does not teach the chemically-mechanically polishing step required by claim 9 for the same reasons outlined for claim 1. With respect to claim 17, the Examiner argued that determining a thickness range is obvious as a routine exercise of skill in the art. Applicant also notes that Doan does not teach the chemically-mechanically polishing step required by claim 17 for the reasons outlined for claim 1. Thus, claims 9 and 17 are patentable over the Doan reference.

New claim 18 recites, in part,

> "chemically-mechanically polishing the layer of second material and the underlying layer of first material until the layer of first material is substantially planar

to form a planarized layer of first material, the planarized layer of first material covering the wafer upper level of the top surface of the wafer."

However, as shown in FIG. 3, Doan teaches that at the end of the second CMP process, the layer of first material (tungsten layer 22) does not cover the wafer upper level (the top surface of dielectric regions 10). Thus, since Doan does not teach that the layer of tungsten covers the top surface of dielectric regions 10 after the second CMP process, claim 18 is not anticipated by Doan. In addition, since claims 19-23 depend directly or indirectly from new claim 18, claims 19-23 are patentable over Doan for the same reasons as new claim 18.

Thus, for the foregoing reasons, it is submitted that all of the claims are in a condition for allowance. Therefore, the Examiner's early re-examination and reconsideration are respectively requested.

Respectfully submitted,

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Dated: 3-15-02 By: _____

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APPENDIX

In the Drawings

Please amend FIG. 3A as shown in red on the attached copy of FIG. 3A to add reference label 321 to represent the top surface of polysilicon layer 320, and reposition label 300.

Please add FIG. 3C as shown in red on the attached copy of FIG. 3C to illustrate the formation of a layer of material 342.

In the Specification

Please amend the fourth paragraph on page 4 to read as follows:

FIGs. 3A-[3B] 3C are cross-sectional drawings illustrating a method for forming a thin, planarized layer of polysilicon in accordance with the present invention.

Please amend the fifth paragraph on page 4 to read as follows:

FIGs. 3A-[3B] 3C show cross-sectional drawings that illustrate a method for forming a thin, planarized layer of polysilicon in accordance with the present invention. As shown in FIG. 3A, the method utilizes a conventionally processed semiconductor wafer 300 that has a top surface 310. Surface 310, in turn, has a number of substantially-equal lower levels 312 and a number of substantially-equal upper levels 314 that lie above the lower levels 312.

Please amend the first paragraph on page 5 as follows:

As further shown in FIG. 3A, the method begins by depositing a layer of polysilicon 320 on surface 310. Polysilicon layer 320 is conformally deposited and, as a result, also has a top surface 321 that has a number of substantially-equal lower levels 322 and a number of substantially-equal upper levels 324 that lie above the lower levels 322.

Please amend the fifth paragraph on page 5 (which continues on to page 6) as follows:

Alternately, after the planarization step, one or more additional layers of materials, such as materials which lower the resistance of polysilicon, can be formed over layer 340. As shown in FIG. 3C, a layer of material 342 that lowers resistance is formed over planarized polysilicon layer 340. The mask is then formed and patterned on the additional layers of material (e.g., layer 342) which are then etched along with planarized polysilicon layer 340 to form the structures (e.g., local interconnect lines). Either way, once the structures have been formed, the method continues with conventional back-end processing steps.

In the Claims

Please cancel claims 3, 4, 8, 11, and 12.

Please amend the claims as follows:

1. (Amended) A method for forming a planarized layer of material on a processed wafer, the wafer having a top surface, the top surface having a wafer lower level and a wafer upper level that lies above the wafer lower level, the method comprising the steps of:

forming a layer of first material on the top surface of the wafer, the layer of first material having a top surface, the top surface of the layer of first material having a first lower level and a first upper level that lies above the first lower level;

forming a layer of second material on the top surface of the layer of [second] first material; and

chemically-mechanically polishing the layer of second material and the underlying layer of first material with a slurry until the layer of second material is all removed from the layer of first material without changing the slurry to form the planarized layer of material.

5. (Amended) The method of claim [4] 2

wherein the planarized layer of [first] material has a thickness over the wafer upper level, and

wherein the layer of first material is formed such that the first lower level lies above the wafer upper level by a value that is equal to or greater than the [minimum] thickness.

13. (Amended) The method of claim [12] 10

wherein the planarized layer of [first] material has a thickness over the wafer upper level, and

wherein the layer of first material is formed such that the first lower level lies above the wafer upper level by a value that is equal to or greater than the [minimum] thickness.

New claims 18-23 have been added.

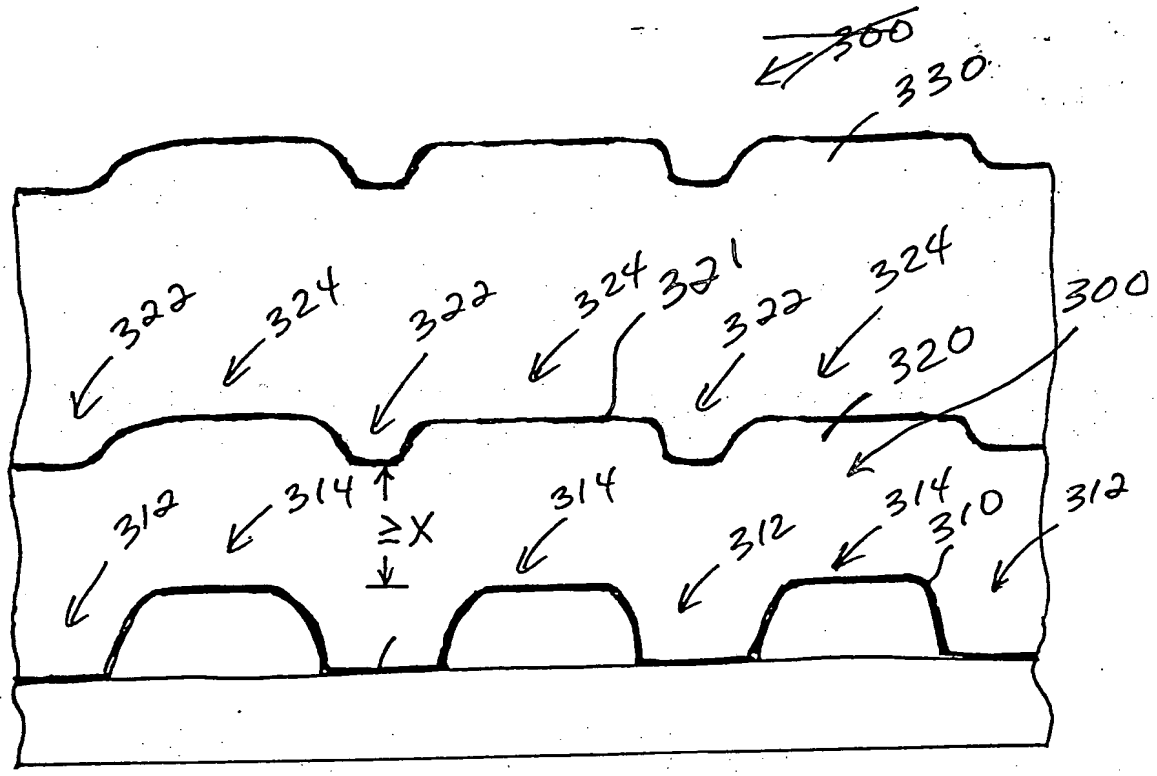

FIG. 3A

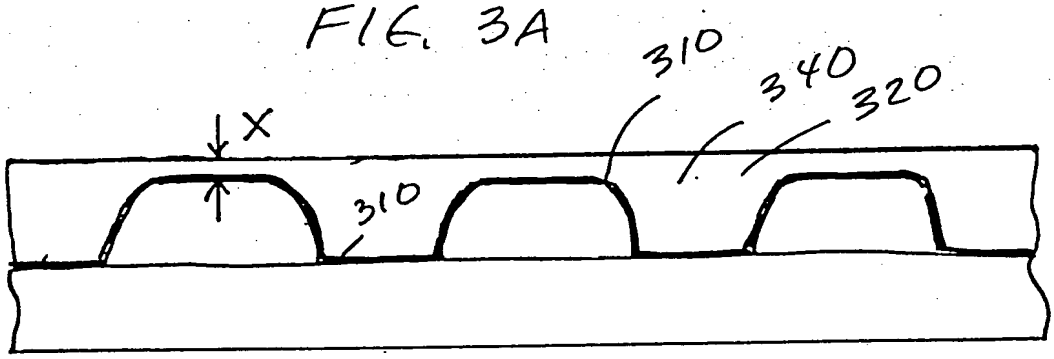

FIG. 3B

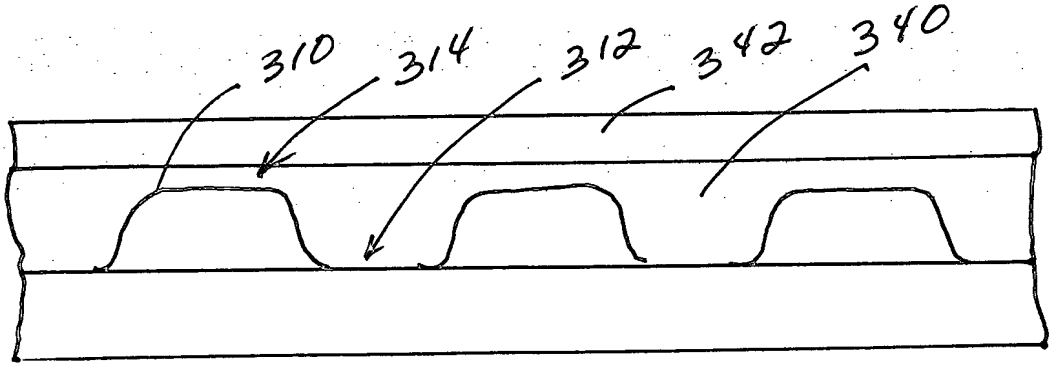

FIG. 3C